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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,432	11/03/2003	Terunao Hanaoka	108086.01	1514

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OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
NGUYEN, KHIEM D	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 04/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/698,432	TERUNAO HANAOKA	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *121603* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-19 are rejected under the judicially created doctrine of double patenting over claims 1-17 of U. S. Patent No. 6,667,551 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows: a method of manufacturing a semiconductor device comprising the steps of: forming a hole in an electrode, the electrode formed on a semiconductor element; forming a through-hole in the semiconductor element so as to be connected to the hole; and forming a conductive layer in a region including an inner side of the through-hole.

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of

the application which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2 and 5-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Eldridge et al. (U.S. Pub. 2001/0015652).

In re claim 1, **Eldridge** discloses a method of manufacturing a semiconductor device comprising: (a) forming a hole in an electrode, the electrode formed on a semiconductor element **(FIG. 3A: 302)**; (b) after the hole is formed in the electrode, forming a through-hole **(FIG. 3A: 306 and 308)** in the semiconductor element so as to be connected to the hole (pages 11-12, paragraphs [0167]-[0168]); and (c) forming a conductive layer **(FIG. 3A: 311, 312, and 315)** in a region including an inner side of the through-hole (page 12, paragraph [0169]).

In re claim 2, **Eldridge** discloses wherein in the (c) step the conductive layer (FIG. 3A: 311, 312, and 315) is formed on at least part of the electrode (pages 11-12, paragraph [0168]-[0169] and **FIG. 3A**).

In re claim 5, **Eldridge** discloses wherein the through-hole is formed in the (b) step by first forming a pinhole of a width smaller than a width of the through-hole, then expanding the pin hole (pages 11-12, paragraphs [0167]-[0169] and **FIG. 3A**).

In re claim 6, **Eldridge** discloses wherein a cavity is formed in the (b) step at a position at which the through-hole is to be formed, then the pinhole is formed by positioning at the cavity (pages 11-12, paragraphs [0167]-[0169] and **FIG. 3A**).

In re claim 7, **Eldridge** discloses wherein the pinhole is formed by a laser beam, then the pinhole is enlarged by wet etching (pages 11-12, paragraphs [0167]-[0169] and **FIG. 3A**).

In re claim 8, **Eldridge** discloses wherein the method further comprising a step of forming an electrical connection portion **(FIG. 3A: 322)** (pages 11-12, paragraphs [0168] and **FIG. 3A**).

In re claim 9, **Eldridge** discloses wherein the electrical portion is formed as part of the conductive layer in the (c) step (pages 11-12, paragraphs [0168] and **FIG. 3A**).

In re claims 10-12, **Eldridge** discloses wherein the method further comprising a step of forming an insulation film on an inner surface of the through-hoe, after the (b) step and before the (c) step, wherein the conductive layer is formed on the insulation film in the (c) step (pages 11-12, paragraphs [0168] and **FIG. 3A**).

In re claim 13, **Eldridge** discloses wherein the insulation film is formed by chemical vapor deposition (CVD) (page 3, paragraph [0038]).

In re claim 14, **Eldridge** discloses wherein the conductive layer is formed by electroless plating (page 3, paragraph [0038]).

In re claim 15, **Eldridge** discloses wherein a catalyst is exposed in at least a region in which the conductive layer is formed, electroless plating (page 3, paragraph [0038]) is performed to extract a conductive material in the exposed region of the catalyst, and the conductive layer is formed from the conductive material (pages 11-12, paragraphs [0168] and **FIG. 3A**).

In re claim 16, **Eldridge** discloses wherein the semiconductor element is a semiconductor chip (pages 11-12, paragraphs [0167]-[0169] and **FIG. 3A**).

In re claim17, **Eldridge** discloses wherein the semiconductor element is part of a semiconductor wafer (pages 11-12, paragraphs [0167]-[0169] and **FIG. 3A**).

In re claim 18, **Eldridge** discloses electrically connecting together the conductive layer of each of upper and lower semiconductor devices (pages 11-12, paragraphs [0167]-[0169] and **FIG. 3A**).

In re claim 19, **Eldridge** discloses cutting the semiconductor wafer into pieces (pages 11-12, paragraphs [0167]-[0169] and **FIG. 3A**).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eldridge et al. (U.S. Pub. 2001/0015652) as applied to claims 1-2 and 5-19 above, and further in view of Nishi et al. (U.S. Patent 4,806,111).

In re claims 3 and 4, **Eldridge** does not explicitly discloses wherein through-hole comprises an edge portion and an intermediate portion of which width is larger than a width of the edge portion and wherein all portions of the intermediate portion are formed at substantially the same width; and the through-hole comprises a tapered portion connecting the edge portion with the intermediate portion.

Nishi discloses wherein through-hole **(FIG. 3: 15G and 15S)** comprises an edge portion and an intermediate portion of which width is larger than a width of the edge portion and wherein all portions of the intermediate portion are formed at substantially the same width; and the through-hole comprises a tapered portion connecting the edge portion with the intermediate portion (col. 3, line 56 to col. 4, line 27 and **FIGS. 3-5**). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Eldridge and Nishi to enable the through-hole of Eldridge to be formed and furthermore to provide a high density multi-electrode connector structure which can engage and disengage a substrate with and from another similar one with a small insertion extraction force (col. 2, lines 38-46).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
April 17, 2004

W. DAVID COLEMAN
PRIMARY EXAMINER